In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 3, lines 1 to 7 as follows:

--The early direct memory access has evolved into several successive versions of centralized transfer controllers and more recently into the transfer controller with hub and ports architecture. The transfer controller with hub and ports architecture is described in U.S. Patent No. 6,496,740 claiming priority from U.K. Patent Application No. 9901996.9 filed April 10, 1999 entitled "TRANSFER CONTROLLER WITH HUB AND PORTS ARCHITECTURE."--

Rewrite the paragraph at page 3, lines 16 to 30 as follows:

--The transfer controller architecture of the ~~TMS330C80~~ TMS320C80 is fundamentally different from a direct memory access in that only a single set of address generation and parameter registers is required. Prior direct memory access units required multiple sets for multiple channels. The single set of registers, however, can be utilized by all direct memory access requestors. Direct memory access requests are posted to the transfer controller via set of encoded inputs at the periphery of the device. Additionally, each of the digital signal processors can submit requests to the transfer controller. The external encoded inputs are called "externally initiated packet transfers" (XPTs). The digital signal processor initiated transfers are referred to as "packet transfers" (PTs). The RISC processor could also submit packet transfer requests to the transfer controller.--

Rewrite the paragraph at page 4, lines 18 to 25 as follows:

--Finally the transfer controller with hub and ports includes a mechanism for queuing transfers up in a dedicated queue memory.

The TMS320C80 transfer controller permitted only ~~was~~ one transfer outstanding per processor at a time. Through the queue memory provided by the transfer controller with hub and ports, processors may issue numerous transfer requests up to the queue memory size before stalling the digital signal processor.--

Rewrite the paragraph at page 7, lines 7 to 23 as follows:

--The transfer controller with hub and ports ~~transfer controller with hub and ports~~ architecture is optimized for efficient passage of data throughout a digital signal processor chip. Figure 1 illustrates a block diagram of the principal features of the transfer controller with hub and ports. It consists of a system of a single hub 100 and multiple ports 111 through 115. At the heart of the hub is the transfer controller with hub and ports hub control unit 109 which acts upon request and status information to direct the overall actions of the transfer controller.--